IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Currently amended) A semiconductor device structure, comprising:

a substrate including at least one recess formed therein; and

a material layer disposed over the substrate and substantially filling the at least one recess, the material layer having a substantially planar surface ~~substantially free of hills and valleys~~, portions of the material layer that cover a surface of the substrate having a thickness of less than about half a depth of the at least one recess.

2. (Withdrawn) The semiconductor device structure of claim 1, wherein the substrate comprises a semiconductor substrate with a surface and the at least one recess comprises at least one trench recessed in the surface of the semiconductor substrate.

3. (Previously presented) The semiconductor device structure of claim 1, wherein the material layer comprises a mask material.

4. (Previously presented) The semiconductor device structure of claim 3, further comprising at least one conductively doped region continuous with a surface of the semiconductor substrate and adjacent the at least one recess.

5. (Withdrawn) The semiconductor device structure of claim 1, wherein the substrate comprises:

a shallow trench isolation structure including a semiconductor device substrate with a surface and at least one trench formed in the surface of the semiconductor device substrate; and

an insulator layer substantially filling the at least one trench and covering the surface of the semiconductor device substrate.

6. (Withdrawn) The semiconductor device structure of claim 5, wherein the insulator layer includes a nonplanar upper surface with at least one peak located substantially above the surface of the semiconductor device substrate and at least one valley located substantially above the at least one trench.

7. (Withdrawn) The semiconductor device structure of claim 6, wherein the material layer comprises a stress buffer layer that substantially fills the at least one valley in the insulator layer.

8. (Withdrawn) The semiconductor device structure of claim 1, wherein the substrate comprises:

a semiconductor device structure including a surface with at least one dual damascene trench formed thereon; and

a conductive layer substantially filling the at least one dual damascene trench and covering the surface of the semiconductor device structure.

9. (Withdrawn) The semiconductor device structure of claim 8, wherein the conductive layer includes a nonplanar upper surface with at least one peak located substantially above the surface of the semiconductor device structure and at least one valley located substantially above the at least one dual damascene trench.

10. (Withdrawn) The semiconductor device structure of claim 9, wherein the material layer comprises a stress buffer layer that substantially fills the at least one valley in the conductive layer.

11. (Previously presented) The semiconductor device structure of claim 1, wherein the substrate comprises a stacked capacitor structure and the at least one recess comprises at least one container recessed in an insulator layer of the stacked capacitor structure.

12. (Previously presented) The semiconductor device structure of claim 11, wherein the material layer comprises a mask material, the mask material substantially filling the at least one container.

13-14. (Canceled)

15. (Currently amended) A semiconductor device structure, comprising:
a substrate including at least one recess formed therein;
an intermediate layer substantially filling the at least one recess and covering a surface of the semiconductor device substrate, the intermediate layer including at least one valley located substantially above the at least one recess; and
a material layer disposed ~~at least partially~~ over the ~~substrate~~ intermediate layer and substantially filling the at least one valley~~so as to at least partially fill the at least one recess~~, the material layer having a substantially planar surface ~~substantially free of hills and valleys~~, portions of the material layer that cover a surface of the intermediate layer having a thickness of less than about half a depth of the at least one valley.

16. (Previously presented) The semiconductor device structure of claim 15, wherein at least one region of the substrate is exposed through the material layer.

17. (Canceled)

18. (Currently Amended) The semiconductor device structure of ~~claim 17~~ claim 15, wherein at least one region of the at least one intermediate layer is exposed through the material layer.

19. (Currently Amended) The semiconductor device structure of ~~claim 17~~ claim 15, wherein the at least one intermediate layer comprises at least one of a mask material, an insulative material, and a conductive material.

20. (Previously presented) The semiconductor device structure of claim 15, wherein the material layer has a thickness that is less than a depth of the at least one recess.

21. (Previously presented) The semiconductor device structure of claim 1, wherein the surface of the material layer is free of abrasive-planarization-induced defects.

22. (Canceled)

23. (Previously presented) The semiconductor device structure of claim 15, wherein the surface of the material layer is free of abrasive-planarization-induced defects.

24. (Canceled)

25. (New) The semiconductor device structure of claim 15, wherein the intermediate layer includes a nonplanar upper surface with at least one peak located substantially above the surface of the semiconductor device substrate and at least one valley located substantially above the at least one recess.

26. (New) The semiconductor device structure of claim 15, wherein the material layer comprises a mask layer.

27. (New) The semiconductor device structure of claim 15, wherein the material layer comprises a stress buffer layer.

28. (New) A semiconductor device structure, comprising:

a substrate including at least one recess formed therein;

an intermediate layer filling a portion of the at least one recess and leaving at least portions of a surface of the substrate exposed through the intermediate layer; and

a material layer disposed over the intermediate layer and substantially filling a remaining portion of the at least one recess, the material layer having a substantially planar surface, the material layer covering a surface of the intermediate layer having a thickness of less than about half a depth of the remaining portion of the at least one recess.

29. (New) The semiconductor device structure of claim 28, wherein the substrate includes at least one peak.

30. (New) The semiconductor device structure of claim 29, wherein the at least one peak is exposed through the intermediate layer.

31. (New) The semiconductor device structure of claim 29, wherein the at least one peak is exposed through the material layer.

32. (New) The semiconductor device structure of claim 29, wherein the at least one peak of the intermediate layer is exposed through the material layer

33. (New) A semiconductor device structure, comprising:

a substrate including at least one recess formed therein;

an intermediate layer at least partially filling the at least one recess and covering a surface of the semiconductor device substrate, the intermediate layer including at least one valley located substantially above the at least one recess; and

a material layer disposed over the intermediate layer and substantially filling the at least one valley, the material layer having a substantially planar surface, the material layer covering a surface of the intermediate layer having a thickness of less than about half a depth of the at least one valley.

34. (New) The semiconductor device structure of claim 33, wherein the at least one valley is located at least partially in the at least one recess.